IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	John T. Moore and David L. Chapek	§	Group Art Unit:	2811
Serial No.:	09/496,794	§		
Filed:	February 2, 2000	§	Examiner:	D. Owens
For:	Trench Isolation for Semiconductor Devices	§	Atty. Dkt. No.:	MICT-0005-D1-US (97-0608)

Box AF
Commissioner for Patents
Washington DC 20231

REPLY TO FINAL OFFICE ACTION MAILED OCTOBER 17. 2001

Sir:

In response to the final office action mailed October 17, 2001, please amend the claims as following and consider the following remarks.

Please amend claims 26 and 31, as follows:

26. (Amended) A semiconductor structure, comprising:

a support;

a first material deposited on said support, the first material having a first etch rate;

a trench formed through the first material and into the support;

a trench filler material deposited in the trench, the trench filler material having an etch rate that is less than 1.2 times the first etch rate; and → means it can be the same, or a fraction

wherein the first material and the trench filler material are etched simultaneously across the trench.

Date of Deposit: 10/31/01
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, Washington DC 20231.
Lisa O'Sullivan
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